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L6	17	(713/189-194.ccls. 380/28-30,242.ccls. 725/25-31.ccls.) and (cam same reconfigur\$)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/10 11:34
L7	1	(713/189-194.ccls. 380/28-30,242.ccls. 725/25-31.ccls.) and ((conditional adj access) same reconfigur\$)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/10 11:40
L8	1799	713/193.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/10 11:40

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L2	243	digital and (state adj machine) and reconfigur\$ and receiver and cam	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/10 10:32

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IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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1 [Hardware/software tradeoffs in a variable word width, variable queue length buffer](#)

[memory](#)

A. C. Parker, A. W. Nagle

 March 1977 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th annual symposium on Computer architecture ISCA '77**, Volume 5 Issue 7

Publisher: ACM Press

Full text available: pdf(401.04 KB)

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This paper describes a buffer memory design which is integratable on a single 40 pin package. The memory consists of four variable word width, variable length queues, address logic, and logic for configuring the data widths and queue lengths. Simple program commands input on the data lines reconfigure the memories when the circuit is in program mode. In data mode, WRITE and READ requests to a particular buffer enable the memory to load and access itself, update its pointers, and check for f ...

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... are equipped with slots for access cards called **Conditional Access** Modules. ... Tier wipes are updates which are sent down to **reconfigure** unsubscribed ...
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